Mercury ECD Electronics Circuit Description
Revision: 2
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1. Applicability

This document applies to Mercury ECD schematic 03-925044-00, Revision C4.

2. Power supplies and grounds

There are four grounds serving the ECD electronics circuitry. Ground 1 is the return for the +5V digital supply. It is connected directly to Ground 4, the unregulated +24V return, at the card edge connector on the Mother board. The analog return is Ground 2, which provides a low-noise return for the ±15V, +5.25V, and -5V supplies. Ground 3 is the reference for analog signal distribution, which carries almost no DC current. All of the grounds must be tied together externally for the board to function properly.

Four RC filters remove noise from the analog power supplies. These consist of R43 with C32, R44 with C29, R45 with C30, and R46 with C31.

3. Digital circuits

One half of U5 decodes bus address information to access latch U7, buffer U6, and dual DAC U8. The latch holds all of the digital control signals for the board, while the buffer transmits the board identification number (02H) to the bus. R47 and R48 allow the inputs of U6 to be pulled high or low for automatic test. The other half of U5 is used only as an inverter.

4. Power converter

A switching regulator, connected in the inverting configuration, generates -50V from the unregulated +24V input. The maximum current drain from the -50V supply is less than 10mA in normal operation. U2 (a TL494) provides all of the functions needed to control the supply: an oscillator, pulse-width-modulation comparator, voltage reference, dual error amplifiers, and output transistors. C4 and R12 set the oscillator frequency to 50kHz, thus applying a 50kHz sawtooth to one input of the pwm comparator. The other input to the comparator is driven by the outputs of both error amplifiers, which are connected in such a way that the amplifier calling for the lower output from the supply dominates. The minimum dead time between output pulses, regardless of the error amplifiers, is set to about 5% by grounding the DT input of U2 (pin 4).

Error amplifier #1, whose inputs are on pins 1 and 2, is used as the primary loop control amplifier. Its inverting input is connected to the +5V±5% reference voltage (pin 14) through R1, and to the output of the supply through R2. Since the noninverting input is

connected to ground, the IC will adjust its duty cycle to drive the inverting input to zero volts also. This will occur only when the output voltage is -50V, since R2 is ten times as large as R1. Feedback from the error amplifier output (U2-3) is taken through C3 and R4, which stabilizes the loop with a very high DC gain. CR8 prevents pin 2 from being driven to such a low voltage that the IC quits functioning properly.

Both output transistors are driven in phase, because the Output Control pin (U2-13) is tied to ground. The emitters of the transistors (pins 9 and 10) are grounded, and the collectors (pins 8 and 11) drive Q1 through R10. R11 speeds the turn-off of Q1 in between pulses. When Q1 is turned on, the +24V supply is connected to L1, causing the current through L1 to ramp upward. As soon as Q1 is turned off, its collector voltage falls rapidly until CR1 turns on, allowing the inductor current to continue flowing. After a number of pulses, C2 charges to the desired output voltage, and the pulse width stabilizes at the value needed to just maintain the output at -50V. R9 damps the ringing of L1 following the turn-off of Q1. C1 and C6 provide the high-frequency pulses of current drawn through Q1.

The inductor current is sensed by R3, and R6 and C5 smooth the resulting voltage pulses before they are applied to the noninverting input of the second error amplifier (U2-16). The voltage at the inverting input (U2-15) is set to 98mV by R7 and R8. If the output of the -50V supply is shorted, the average current through R3 can rise only to about 21mA before the second error amplifier output rises abruptly, reducing the conduction duty cycle and limiting the output current. R5 provides positive feedback for "foldback" limiting, allowing the average inductor current to reach about 70mA as long as the output voltage is at -50V.

R13 and R14 divide the output voltage of the -50V supply by 51 for measurement by the system ADC through P1-3.

5. Current-to-frequency converter

The circuitry across the top of the schematic page, including the sections labeled ECD ELECTROMETER, V TO F CONVERTER, and ECD PULSER, forms a feedback loop with the external electron capture detector cell. We will begin the description of this circuitry in the middle, where AR2 and AR3 comprise a current-to-frequency converter.

Feedback capacitor C22 configures amplifier AR2 as an integrator, so a constant current into the collector of Q4 causes a rising, linear ramp at the output of AR2 (pin 6). The noninverting input of comparator AR3 is biased to +3V by R26 and R34. Since the ramp voltage from AR2 is applied to the inverting input of AR3 through R33, the output of the comparator (pin 7) will switch from high to low when the ramp voltage reaches 3V. CR5 and CR6 provide hysteresis, ensuring that the comparator output stays low until the ramp has been reset to zero volts. The output of AR3 is an open-collector transistor, so R25 is needed to pull the output up to 5V when the transistor turns off.

When the comparator output switches low, Q5 is turned on, discharging C22 and resetting the ramp. R31 keeps Q5 turned on until the ramp voltage has fallen all the way to ground. The bias current flowing into pin 2 of AR2 (typically 150nA) would keep the current-to-frequency converter running at about 500 pulses per second even if the collector current of Q4 were zero. R30 sources enough current into the amplifier input node to cancel the input bias current, so that the operating frequency can go below 500Hz in all cases.

6. Pulser

Each time the output of comparator AR3 switches from high to low, one-shot U4 generates a positive pulse at pin 13. R24 and C12 set the pulse width to 640ns. Buffer U1 has its individual sections tied in parallel to provide the large drive currents needed to charge the gate capacitances of Q2 and Q3. In between pulses, the outputs of U1 are at ground, and the gate voltage of Q2 is held at -4.5V by R16 and R18. Since Q2 is a p-channel MOSFET, it is turned on when the gate is negative, and the pulser output at J2 is equal to the source voltage at pin 1 of Q2. Q3 (an n-channel device) is turned off during this time, since R20 holds its gate at the same voltage as its source (-50V).

When a pulse from the current-to-frequency converter causes the outputs of U1 to switch to +5V, the gate voltages of both FETs rise by about 5V. Q2 turns off while Q3 turns on, pulling the pulser output to -50V. R19 improves the settling time of the output pulse. C7 forces the gate voltage of Q2 to switch rapidly, while C11 allows the DC voltages at U1 and at the gate of Q3 to be different. CR2 clamps the negative excursions of Q3's gate voltage to the -50V supply, so that the FET continues to be turned on hard even at high pulse frequencies, where it may be on more than 50% of the time.

7. DACs

Detector operation requires the pulser output to have a variable DC offset, which is provided by one half of a dual DAC (U8). AR5 (pins 1-3), R50, and R51 invert the +10V reference, supplying -10V at U8-4 and U8-18. AR5 (pins 8-10) converts the output current of the DAC to a voltage, which varies from 0 to +9.96V as the digital code written to the DAC varies from 0 to 255. To find the voltage at AR6-3, note that R52 is connected to the inverting input of AR6 (pin 6), which remains at a virtual ground potential. R15 offsets the voltage at AR6-3 down by about half the output range of the DAC, resulting in a voltage range of -769mV to +763mV as the DAC setting is varied from 0 to 255. AR6 (pins 1-3) provides a low-impedance output to drive the pulser, and R17 and C8 keep the high-frequency pulser currents out of the amplifier's output. At the highest pulse frequencies, the DC current flowing through R17 can cause as much as 100mV of drop, especially when driving high capacitances at the pulser output.

The other half of dual DAC U8 operates in exactly the same way, generating a voltage between 0 and +9.96V at AR5-7. In normal operation, analog switch U3 (pins 14 and 15)

is open, and the DAC output voltage appears at the bottom end of R27. (The effect of R49 is negligible in series with R27, which is 50,000 times larger.)

8. Electrometer

The other end of R27 is tied to the inverting input of AR1, which must stay at ground (equal to the noninverting input voltage) for the amplifier to function linearly. This means that a current between 0 and 2nA must flow through R27 into the summing junction at AR1-2. Since the input current of AR1 is only a few femtoamps (1fA = 1E-15A), and no DC current can flow through the capacitors connected to AR1-2 , all of the current supplied by the DAC through R27 must flow out through the ECD input connector. The pulser output is normally connected to an electron capture detector (ECD) cell, which draws a small charge from the ECD input through J1 with each pulse. As the composition of the gas in the cell changes, the magnitude of the charge varies, and the circuitry on this board adjusts the pulse frequency to exactly balance the current set by the DAC with the current from the cell.

The electrometer amplifier (AR1) is configured as an integrator by feedback capacitor C16, so any imbalance between the input currents from the ECD cell and R27 at pin 2 causes the output voltage at pin 1 to slew up or down in response. The idealized output voltage should therefore be a linear ramp downward due to the constant current from the DAC, with sudden rises in voltage when the pulses occur. Because there is a large capacitive feedthrough of the pulse through the cell, which is much faster than the amplifier can follow, there is a large glitch in the amplifier output at each pulse. C15 helps to absorb these rapid changes in current, but the output waveform of AR1 is dominated by the glitches, which obscure the idealized waveform at frequencies above a few kilohertz. R35 and C17 smooth the output waveform further.

9. Exponential gain compensation

When the instrument is operating at baseline conditions, a relatively large charge is delivered with each pulse, resulting in a pulse frequency of about 1.6kHz. As the delivered charge per pulse decreases, the frequency may rise as high as several hundred kilohertz to keep the average current constant. The gain of the feedback path thus varies in inverse proportion to the pulse frequency, since the charge per pulse must be inversely proportional to the pulse rate in order to maintain constant average current.

In order to keep the feedback loop gain constant as the pulse frequency changes, an element must be introduced into the circuit whose output varies exponentially with its input. The collector current of a bipolar transistor varies exactly this way with respect to its base-emitter voltage. The filtered output of the electrometer is buffered by AR1 (pins 5-7) to provide a low-impedance drive for the emitter of Q4. Since the collector current of Q4 drives the current-to-frequency converter, and both the transconductance of Q4 and the pulse frequency are proportional to the collector current, the desired compensation is achieved.

CR7 and R29 limit the maximum frequency which can be set for the current-to-frequency converter. Frequency settings which approach or exceed the reciprocal of the pulse width (1.6MHz) would cause irregular pulse intervals, which must be avoided.

10. Diagnostic feedback circuit

Because the electrometer is configured as an integrator, its output will inevitably swing to one of the power supply rails if a feedback current (proportional to pulse frequency) is not applied to its input. Such a feedback source is provided on the board, so the board may be tested without having an external connection to an ECD cell. To enable this diagnostic feature, analog switch U3 (pins 14 and 15) is closed and switch section U3 (pins 2 and 3) is opened. The output pulses are "stretched" by CR4 and C38, and then summed with the Cell Current DAC output through R49 and R22. Since the average voltage at the bottom end of R27 must remain at zero volts for the integrating electrometer to function, the circuit will adjust the pulse frequency to make the average voltage at the anode of CR4 equal to the opposite of the voltage at AR5-7. Linearity of the diagnostic circuit is improved by C39, which absorbs the pulses without letting the voltage rise significantly. R23 holds the voltage at U3 (pins 2 and 14) below -15V even at the highest frequencies, but has no effect on the operating point of the loop, since it has no DC voltage across it. Stretching the pulses allows operation at lower frequencies at the desired voltage levels from the Cell Current DAC.

11. Output amplifier

The information from the electron capture detector is contained in the pulse frequency, so this frequency is converted to a voltage for system use. The output pulse stream is averaged by R21 and C21. Since the DC offset applied to the pulser output carries no signal information, its effect must be removed from this averaged signal. The offset voltage, which appears at AR6-3, is inverted by AR6 (pins 5-7), R52, and R36. Because R41 is equal to R21, the inverted voltage from AR6-7 cancels the pulser DC offset voltage, which appears at J2-1 between pulses. AR4 amplifies the averaged pulse signal, with C20 providing further smoothing. Resistor R40 can be paralleled with feedback resistor R37 through U3 (pins 6 and 7) to select one of two gains for the output amplifier. R42 adds an offset to the signal, so the normal resting frequency of 1.6kHz produces zero output voltage at AR4-6. R39 and C28 prevent glitches from the system ADC input multiplexer from disturbing AR4.

12. Log of revisions and file identification

Rev. 1 7/27/95

Rev. 2 3/18/96 Main changes:

Pulser DC offset circuit and output amplifier input offset circuit descriptions (Sections 7 & 11) changed to reflect circuit changes in Rev. C4.

File: ENGRSERV:\3800ELEC\DOC\ECDCD.DOC

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